UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/604,910	08/26/2003	Stephen F. Geissler	BUR920020054US1	1909

31647 7590 08/25/2004

DUGAN & DUGAN, P.C.
55 SOUTH BROADWAY
TARRYTOWN, NY 10591

EXAMINER	
ENGLUND, TERRY LEE	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 08/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/604,910	GEISSLER, STEPHEN F.	
	Examiner	Art Unit	
	Terry L Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Aug 26, 2003 & May 18, 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 12-20* is/are rejected.

7)☒ Claim(s) *4-11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 August 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *05182004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: P1-P2, N1-N2, D1-D2, and R are never described in the disclosure. Therefore, it is suggested these reference characters be removed from each of Figs. 1-4 because all the elements are identified in the figures, and the disclosure, by corresponding numerical references. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The abstract of the disclosure is objected to because it does not describe how the first and second NFETs are actually related to one another. It is suggested the abstract indicate these two transistors form a current mirror type configuration. Correction is required. See MPEP § 608.01(b).

Claim Objections

Claims 15-19 are objected to because of the following informalities: To minimize possible confusion, consistent labeling should be used throughout the claims. Therefore, it is suggested --circuit-- be added after "reference" on line 1 of claim 15. Dependent claims 16-19 carry over the objection from claim 15. An appropriate correction is required.

Claim Rejections - 35 USC § 112

Claims 1-3, and 20 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: how the first and second NFETs actually relate to one another. For example, as presently written, those two NFETs could be coupled in series or parallel, or just be two separate NFETs that happen to be configured in what can be deemed a current reference circuit.

Dependent claims carry over any rejection(s) from any claim(s) upon which they depend.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 12, 14-17, and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by the applicant's own Prior Art Fig. 2. The figure shows current reference circuit 200 comprising first NFET 106 having its gate and drain coupled together, and second NFET 108. Since NFET 108 of Fig. 2 is represented by the same exact symbol as NFET 108 in the applicant's Fig. 4, which is clearly disclosed as having its body left floating (i.e. see the last two lines of paragraph 0020), it is understood second NFET 108 in Fig. 2 also has a floating body. Therefore, claim 1 is anticipated. Since Fig. 2 is clearly disclosed as a conventional current reference circuit, one of ordinary skill in the art would understand the circuit generates a reference current within at least one of the first/second NFETs. Since first NFET 106 has its gate and drain coupled together, and second NFET 108 has a floating body, claim 12 is anticipated. Referring to current reference circuit 200 of Fig. 2, the gates of first/second NFETs 106/108 are coupled together; first NFET 106 has a grounded source, and the source of second NFET 108 is coupled to ground via resistive element 110; first PFET 102 has its drain coupled to the drain of first NFET 106, its source coupled to supply voltage VDD, and its gate coupled to the gate of second PFET 104, which has its drain coupled to the drain of second NFET 108, and its source coupled to supply voltage VDD. Thus, claims 14-16 are anticipated. With second NFET 108 having a floating body, the Fig. 2 circuit could be used with a 0.5 volt supply voltage to drive the current reference circuit, and claims 17 and 20 are anticipated.

Claims 1, 12, 14-16, and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Kobatake. Fig. 7 of Kobatake shows a current reference circuit comprising elements that closely correspond to the applicant's own Fig. 6. For example, Kobatake's P1, P2, P4, P5, N3, N4, N1, N2, and R1 basic structure corresponds to 102, 104, 602a, 602b, 604a, 604b, 106, 108, and 110

of current reference circuit 600 shown in the applicant's Fig. 6. Therefore, the current reference circuit of Kobatake comprises first NFET N1 with its gate and drain coupled together, and second NFET N2 with a floating body, anticipating claim 1. [Note: The "floating body" reasoning is based on: 1) Since Kobatake neither shows nor discloses the connections of N2's body, it is assumed each body is floating. And, 2) Only the body of first NFET 106 of the applicant's own Figs. 3, 4, and 6 is clearly shown coupled to ground; the body of second NFET of the applicant's own Fig. 3 is clearly shown coupled to ground; and none of the other transistors within any of the figures are shown with a body connection. Since the present application's paragraph 0020 discloses that the "body of the second NFET 108 is left floating (as shown)", it must be assumed each of the other transistors (with no specific connection shown or disclosed) also has a floating body.] Interpreting the current reference circuit of Fig. 7 in a slightly different manner, one of ordinary skill in the art would understand it provides reference currents I1/I2 within first/second NFETs N1/N2, respectively. Therefore, claim 12 is anticipated. The coupled gates of first/second NFETs N1/N2 anticipate claim 14. First NFET N1 is shown with a grounded source, and the source of second NFET N2 is coupled to ground via resistive element R1, anticipating claim 15. The figure also shows first PFET P1 with its drain coupled to the drain of first NFET N1 via P4,N3, and a source coupled to supply voltage Vdd; and second PFET P2 with its gate coupled to the gate of first PFET P1, its drain coupled to both the drain of second NFET N2 via P5,N4 and the gate of second PFET P2, and its source is coupled to supply voltage Vdd, anticipating claim 16. Third NFET N3, fourth NFET N4, first PFET P4, second PFET P5, third PFET P1, and fourth PFET P2 anticipate claim 18. [Note: Since the structure of Kobatake's Fig. 7 corresponds to the applicant's own Fig. 6 current reference circuit as

previously described, it is not necessary to describe all of the specific connections (e.g. gate, drain, and source) here.]

Claims 1, 12-13, and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Cable et al. (Cable). Fig. 3 shows what can be considered one type of current reference circuit. It comprises first NFET M5 with its gate and drain coupled together, and second NFET M1 with a floating body (e.g. see paragraph 0031 and "electrically floating"), anticipating claim 1. Interpreting the circuit in a slightly different manner, circuit 3 provides a current reference circuit having first NFET M5 with its gate and drain coupled together, and second NFET M1 with a floating body, wherein one of ordinary skill in the art can consider the current flowing through first NFET M5 as one type of reference current, thus claim 12 is anticipated. Since Cable associates the circuit to silicon-on insulator (e.g. see the abstract and paragraphs 0012 and 0061-0062), first/second NFETs M5/M1 can be silicon-on-insulator FETs, anticipating claim 13. Cable discloses, in at least paragraph 0017, that the operating voltages can be as "low as 0.2 V." Therefore, claim 20, and its "supply voltage of not more than about 0.5 volts", is anticipated

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's own Prior Art Fig. 2 as applied to claim 12 above. As previously described, Fig. 2 shows a current reference circuit that is understood to generate a reference current within at least one of

first/second NFETs 106/108. However, the description of the prior art circuit does not clearly disclose the transistors comprise silicon-on-insulator FETs. It would have been obvious to one of ordinary skill in the art to form all four of the transistors of the applicant's current reference circuit 200 by using silicon-on-insulator field effect transistors, thus rendering claim 13 obvious. The SOI structure is one known means for isolating complementary MOS transistors from a substrate to minimize possible latch-up paths, as well as to eliminate inherent parasitic circuit elements due to junction capacitances between adjacent components. Since circuit 200 comprises two NFETs (i.e. 106 and 108) and two PFETs (i.e. 102 and 104), forming them in an SOI structure would have been obvious as described above.

Claims 13 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kobatake as applied to claims 12 and 18 above. Although Fig. 7 of Kobatake shows/discloses a current reference circuit comprising the first/second NFETs as recited within claim 12; the resistive element of claim 15; and the third-fourth NFETs and first-fourth PFETs as recited within claim 18, the reference does not clearly show or disclose the transistors comprising silicon-on-insulator (SOI) FETs, or the use of a 3.3 volt supply voltage to drive the current reference circuit. It would have been obvious to one of ordinary skill in the art to form all of the transistors of Kobatake's circuit using silicon-on-insulator field effect transistors, thus rendering claim 13 obvious. The SOI structure is one known means for isolating complementary MOS transistors from a substrate to minimize possible latch-up paths, as well as to eliminate inherent parasitic circuit elements due to junction capacitances between adjacent components. Since Kobatake's circuit comprises four NFETs (i.e. N1-N4) and at least four PFETs (i.e. P1-P2, P4-P5), forming the transistors in an SOI structure would have been obvious as previously

described. It also would have been obvious to one of ordinary skill in the art to provide 3.3 volts as supply voltage Vdd of Kobatake's circuit, thus rendering claim 19 obvious. Even if each transistor, within a current path comprising four series coupled transistors (e.g. P1, P4, N3, N1), has a threshold voltage of 0.7 volts, the circuit could conceivably operate using a 2.8 volts supply voltage. However, since resistive element R1 would also drop some voltage with respect to the series coupled transistor path of P2, P5, N4, N2, a slightly higher supply voltage could be used. Supply voltages of 3.0 and 3.3 volts are common, and thus well known to one of ordinary skill in the art. Therefore, either supply voltage could be used to drive the current reference circuit of Kobatake. The 3.0 and 3.3 volts can both be considered "about a 3.3 volt supply voltage."

No claim is allowable as presently written.

Allowable Subject Matter

However, claims 2-3 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims. There is presently no motivation to modify or combine any prior art reference(s) to ensure the first NFET has a body coupled to ground, and a second NFET with a floating body, as claim 2 recites. However, the structural relationship(s) between the first and second NFETs must first be clarified. Claim 3 depends on claim 2.

Claims 4-11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claim 4 relates the first and second NFETs together by clearly indicating their gates are coupled together, and there is presently no motivation to have the body

of the first NFET grounded, wherein the body of the second NFET is floating in such a configuration. Claims 5-11 depend on claim 4.

Prior Art

The other prior art references cited on the accompanying PTO-892 are deemed relevant to at least sections of the claimed invention. Elements 12, 14, 18, 20, and 24 of Zhou et al.'s Fig. 1 directly correspond to elements 102, 104, 106, 108, and 110 of the applicant's own Prior Art Fig. 2, and, other than lacking the body connections of NFETs 18/20, closely correspond to the first current reference circuit 400 shown in the applicant's Fig. 4. However, instead of having a floating body, NFET 20 of Zhou et al. is disclosed as being coupled to ground (i.e. see column 5, lines 41-42). Fig. 3 of Yamazaki also closely corresponds to the applicant's own first current reference circuit 400 shown in Fig. 4. However, in Yamazaki's circuit, each transistor body is clearly shown with a corresponding connection. For example, the body of second NFET 112 is shown coupled to ground. Therefore, neither of these references shows or discloses the two NFETs with the first NFET having its body coupled to ground and the second NFET having its body left floating as at least claim 2 recites.

The prior art references cited on the IDS submitted May 18, 2004 were reviewed and considered. None of these references clearly shows or discloses the body of an NFET as floating.

Any inquiry concerning this communication from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (571) 272-1740.

The new central official fax number is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLE

Terry L. Englund

11 August 2004

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800